Arasan Chip Systems Announces ONFI 3.0 NV-DDR2 PHY

SAN JOSE, Calif., Sept. 30, 2011 (GLOBE NEWSWIRE) — Arasan Chip Systems, Inc. (“Arasan”), a leading provider of Total IP Solutions, announced today that the company added an ONFI 3.0 PHY to its Flash Storage solution. Arasan’s existing ONFI 3.0 NAND Flash Controller with patent pending dynamically configurable ECC technology seamlessly integrates with the new PHY to form an easy to use, high-performance Flash Storage solution. As the NAND Flash landscape is changing, Arasan NAND Flash Controller IP Core is changing with it. The increasing demand for NAND flash with higher data transfer rates and better data integrity has led to the creation of the ONFI 3.0 NAND flash specification supporting 400MT/sec.

Compliant to the ONFI 3.0 electrical interface, Arasan’s ONFI 3.0 PHY, is designed to be delivered as a GDS II hard macro, and is process technology proven and easy to integrate. This ONFI 3.0 PHY, supporting NV-DDR2 up to 400MT/s with capability of scaling speed, accelerates time-to-market by reducing SoC designers’ development time otherwise spent on ensuring high speed signal integrity. Many memory subsystem digital designers have experienced tremendous challenges with ever increasing data transfer rates and differential signaling. Robust memory subsystem bus design with very high signal integrity and low noise ratio usually requires dedicated and experienced analog circuit designers. By using Arasan’s solution, SoC designers can now confidently and easily integrate the ONFI 3.0 PHY into their SoC’s with high success rate of first-time working silicon with high ONFI 3.0 data rates.

Focusing on high performance and high reliability, Arasan’s previously announced ONFI 3.0 NAND Flash Controller IPis designed with Arasan’s patent pending ECC engine with dynamically configurable code-length Bose-Chaudhuri-Hocquenghem (BCH) coders and decoders for high performance and high data rate error corrections. The patent pending configurable code-length BCH coders and decoders perform the Inversion-less Berlekamp-Massey Algorithm (IBMA) to generate or decode ECC codes on each clock. With Arasan’s innovative code-length configurability, from 1-bit to 32-bits, the BCH coders and

decoders can match the target NAND flash error correction requirements; the number of clocks required to generate or decode ECC codes are greatly reduced, thus increasing system performance. In addition, configurable code-length matching for the target NAND ECC requirement (for example 24-bit ECC) eliminates unnecessary waste of ECC code storage area (i.e. NAND spare area) when compared to using a fixed-code-length ECC engine. With the short code-length in this example, Arasan's NAND Flash Controller provides the flexibility to use NAND flash with smaller spare area, or to free up the spare area for other purpose.

"We are very pleased to continue adding to our PHY and patent portfolio as a result of our commitment to invest in a Total IP Solution approach," said Andrew Haines, Sr. Director of Worldwide Marketing. "With our deep domain knowledge in interface standards accumulated in the past 15 years and with inputs from more than 300 global customers, we have invested in developing total IP solutions which include digital IP, PHY, verification IP, software stack, hardware development platform (HDP), electronic system level verification (ESL), and engineering support, for easy and seamless SoC integration. The ONFI 3.0 PHY and the dynamically configurable ECC technology make the adoption of latest ONFI 3.0 standard significantly easier for SoC engineers."

Arasan's ONFI 3.0 NAND Flash Controller IP supports SLC and MLC NAND up to 128Gb NAND flash, synchronous and asynchronous NAND interfaces, page size of 512B, 2KB, 4KB, and 8KB, BCH error correction up to 64-bit ECC, and eight chip-selects.

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